

Notice of Allowability

Application No.

09/912,596

Examiner

Kevin M. Nguyen

Applicant(s)

KOYAMA, JUN

Art Unit

2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/12/04.
2. ☒ The allowed claim(s) is/are 3-7,20,22,23,25,26,28,29,31,32,34,35,37,38 and 44-63 renumbered as claims 1-38.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☒ including changes required by the ~~attached Examiner's Amendment/Comment or~~ in the Office action of ~~Paper No./Mail Date 10/23/2003~~.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
~~Paper No./Mail Date 10/12/04~~
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


XIAO WU
PRIMARY EXAMINER

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/12/2004 has been entered. An action on the RCE follows:

REASONS FOR ALLOWANCES

2. Claims 3, 5, 6, 22, 25, 28, 31, 34, 37, 44, 4, 7, 20, 23, 26, 29, 32, 35, 38, 45, 46, 48, 49, 52, 54, 56, 58, 60, 62, 47, 50, 51, 53, 55, 57, 59, 61, 63 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Okumura et al teaches an EL display device including a source signal line (411), n writing and reading gate signal lines (412), n writing transistors (426), n reading transistors (427), n x m memory circuits (PM1, PM2), n writing memory circuit selection portions (421), n reading memory selection portions (422) (see figures 21 and 25, column 24, lines 26-45, column 26, lines 32-48 and column 29, lines 4-11).

Accordingly, the cited prior arts do not teach or fairly suggest an independent claim 3, an electroluminescence display (EL) device including

a source signal line, n (n is a natural number, $n \geq 2$) writing gate signal lines, n reading gate signal lines, n writing transistors, n reading transistors, n x m memory circuits for storing n-bit digital signals for m frames (m is a natural number, $m \geq 1$), n

Art Unit: 2674

writing memory circuit selection portions, n reading memory circuit selection portions, a current supply line, an EL driving transistor, and an EL element, wherein:

gate electrodes of said n reading transistors are electrically connected to different ones of said n reading gate signal lines, one of a source region and a drain region of each of said n reading transistors is electrically connected to different signal output portions of said n reading memory circuit selection portions, the other of the source region and the drain region of each of said n reading transistors is electrically connected to a gate electrode of said EL driving transistor, one of a source region and a drain region of said EL driving transistor is electrically connected to said current supply line, and the other of the source region and the drain region of said EL driving transistor is electrically connected to one electrode of said EL element.

An independent claim 4, an electroluminescence display (EL) device including

n (n is a natural number, $n \geq 2$) source signal lines, a writing gate signal line, n reading gate signal lines, n writing transistors, n reading transistors, n x m memory circuits for storing n-bit digital signals for m frames (m is a natural number, $m \geq 1$), n writing memory circuit selection portions, n reading memory circuit selection portions, a current supply line, an EL driving transistor, and an EL element, wherein:

gate electrodes of said n reading transistors are electrically connected to any different one of said n reading gate signal lines, one of a source region and a drain region is electrically connected to different signal output portions of said n reading memory circuit selection portions, the other of the source region and the drain region of each of said n reading transistors is electrically connected to a gate electrode of the EL

Art Unit: 2674

driving transistor, one of source region and a drain region of said EL driving transistor is electrically connected to said current supply line, and the other of the source region and the drain region of said EL driving transistor is electrically connected to one electrode of said EL element.

An independent claim 46, an electroluminescence display (EL) device including

a source signal line, n (n is a natural number, $n \geq 2$) writing transistors, n reading transistors, $n \times m$ memory circuits for storing n -bit digital signals for m frames (m is a natural number, $m \geq 1$), n writing memory circuit selection portions, n reading memory circuit selection portions, a current supply line, an EL driving transistor, and an EL element, wherein:

one of a source region and a drain region of each of said n reading transistors is electrically connected to different signal output portions of said n reading memory circuit selection portions, the other of the source region and the drain region of each of said n reading transistors is electrically connected to a gate electrode of said EL driving transistor, one of a source region and a drain region of said EL driving transistor is electrically connected to said current supply line, and the other of the source region and the drain region of said EL driving transistor is electrically connected to one electrode of said EL element.

An independent claim 47, an electroluminescence display (EL) device including

n (n is a natural number, $n \geq 2$) source signal lines, n writing transistors, n reading transistors, $n \times m$ memory circuits for storing n -bit digital signals for m frames (m is a natural number, $m \geq 1$), n writing memory circuit selection portions, n reading memory

Art Unit: 2674

circuit selection portions, a current supply line, an EL driving transistor, and an EL element, wherein:

one of a source region and a drain region is electrically connected to different signal output portions of said n reading memory circuit selection portions, the other of the source region and the drain region of each of said n reading transistors is electrically connected to a gate electrode of the EL driving transistor, one of source region and a drain region of said EL driving transistor is electrically connected to said current supply line, and the other of the source region and the drain region of said EL driving transistor is electrically connected to one electrode of said EL element.

These distinct features have been added to the independent claims and render the above limitations are allowable.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

Art Unit: 2674

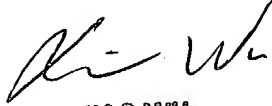
(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

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November 23, 2004


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